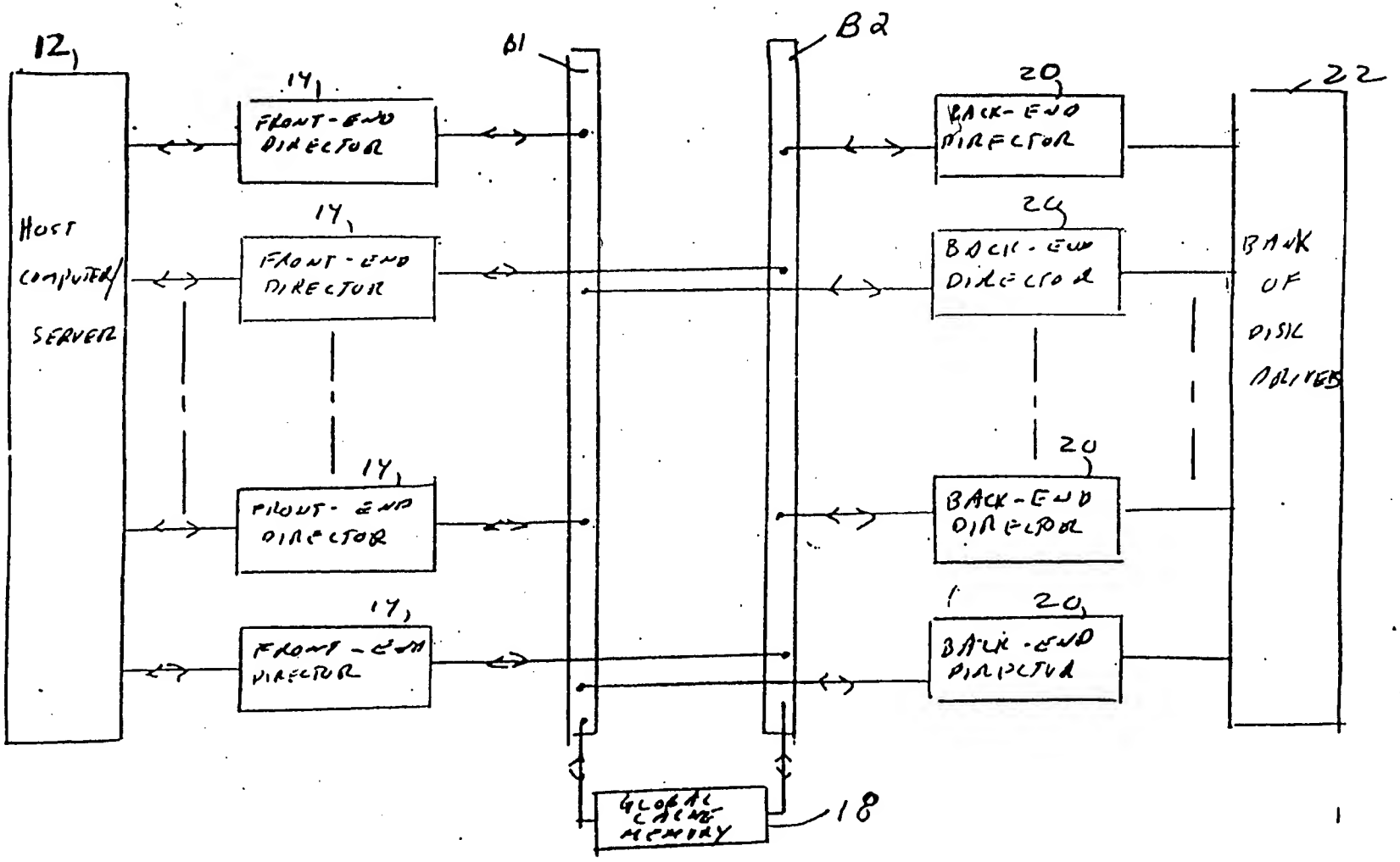
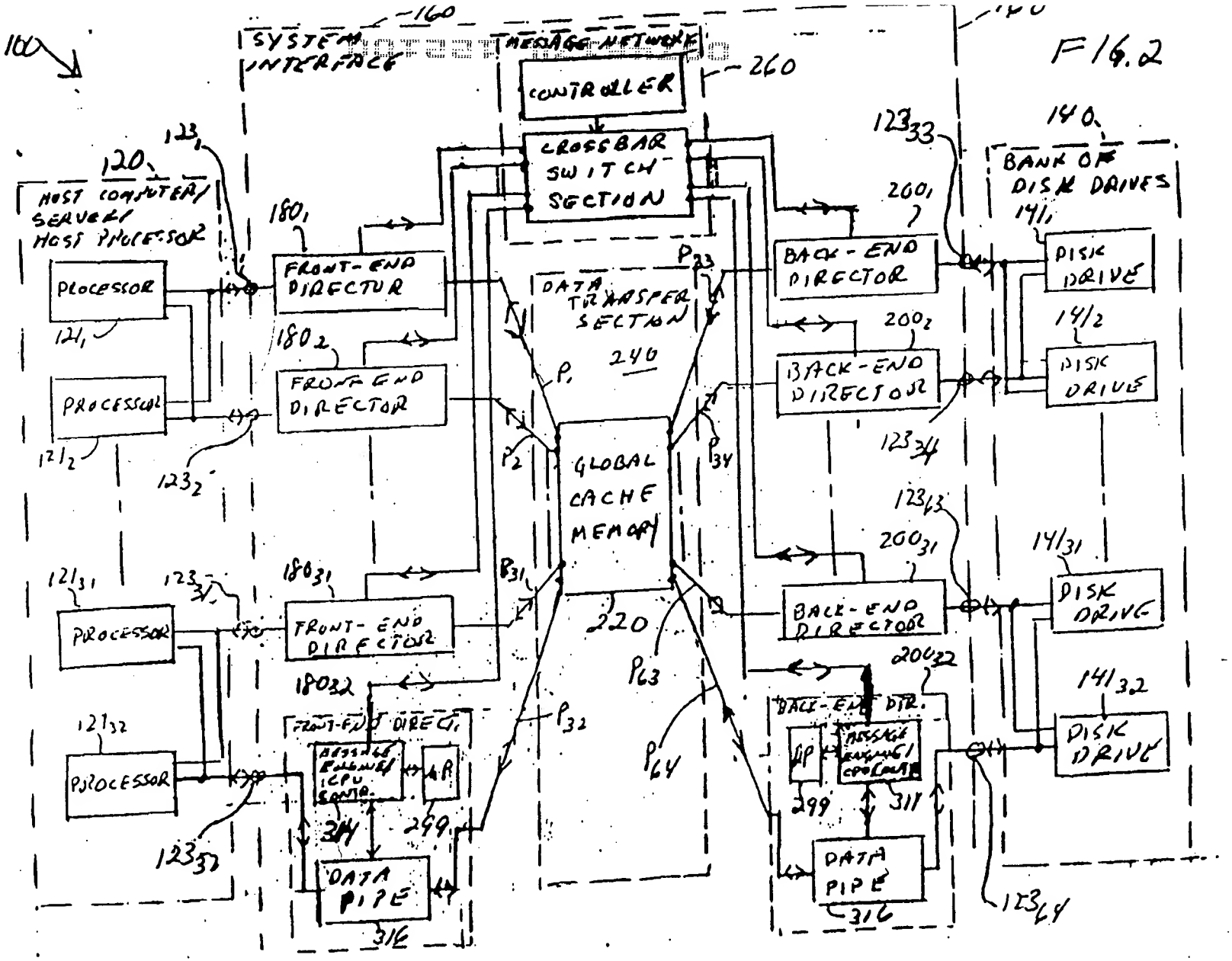
FIG. 1
PRIOR ART




100
SYSTEM INTERFACE
160
MESSAGE NETWORK
CONTROLLER
260
CROSSBAR SWITCH SECTION
120
HOST COMPUTER/ SERVER/ HOST PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
121
FRONT-END DIRECTOR
FRONT END DIRECTOR
FRONT-END DIRECTOR
DATA TRANSFER SECTION
240
GLOBAL CACHE MEMORY
220
BACK-END DIRECTOR
BACK-END DIRECTOR
BACK-END DIRECTOR
BACK-END DIR.
140
BANK OF DISK DRIVES
DISK DRIVE
DISK DRIVE
DISK DRIVE
DISK DRIVE
DATA PIPE
DATA PIPE
316
299
311
P1
P2
P31
P32
P33
P34
P63
P64

F16.2

16/64

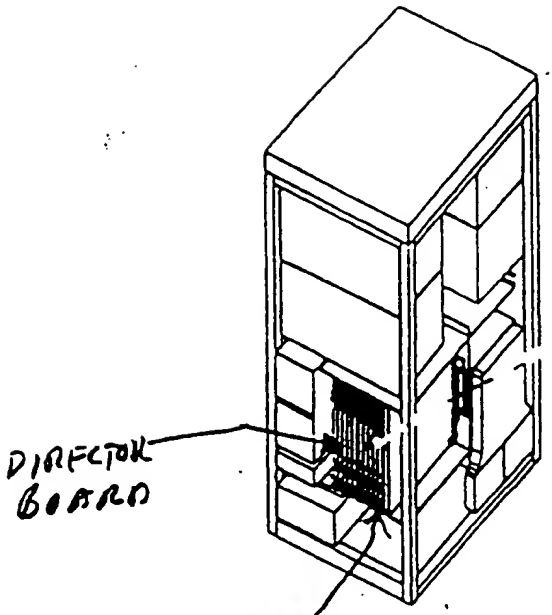
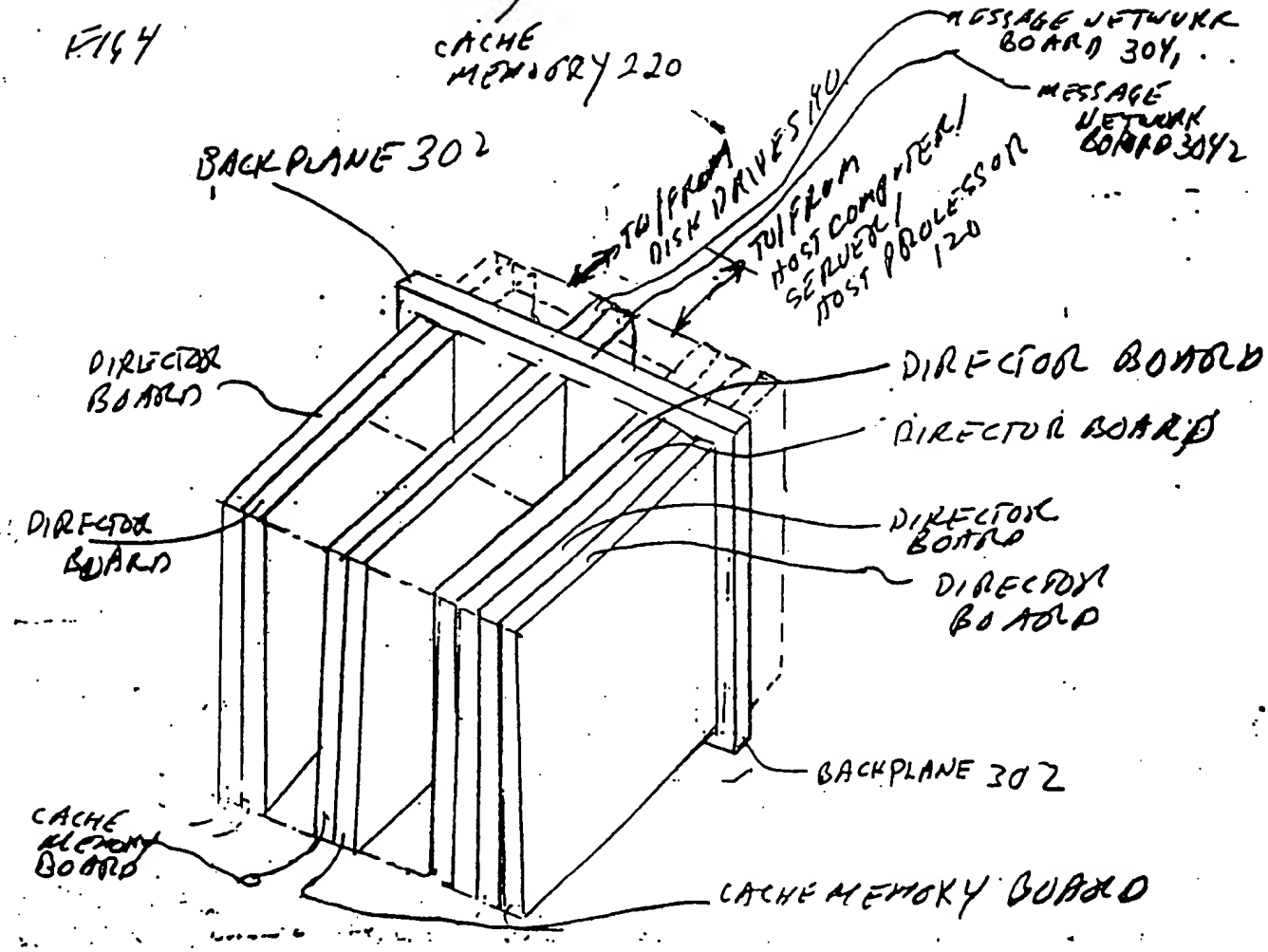

DIRECTOR BOARD
CACHE MEMORY 220

FIG. 3

FIG 4


MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304 2
BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD

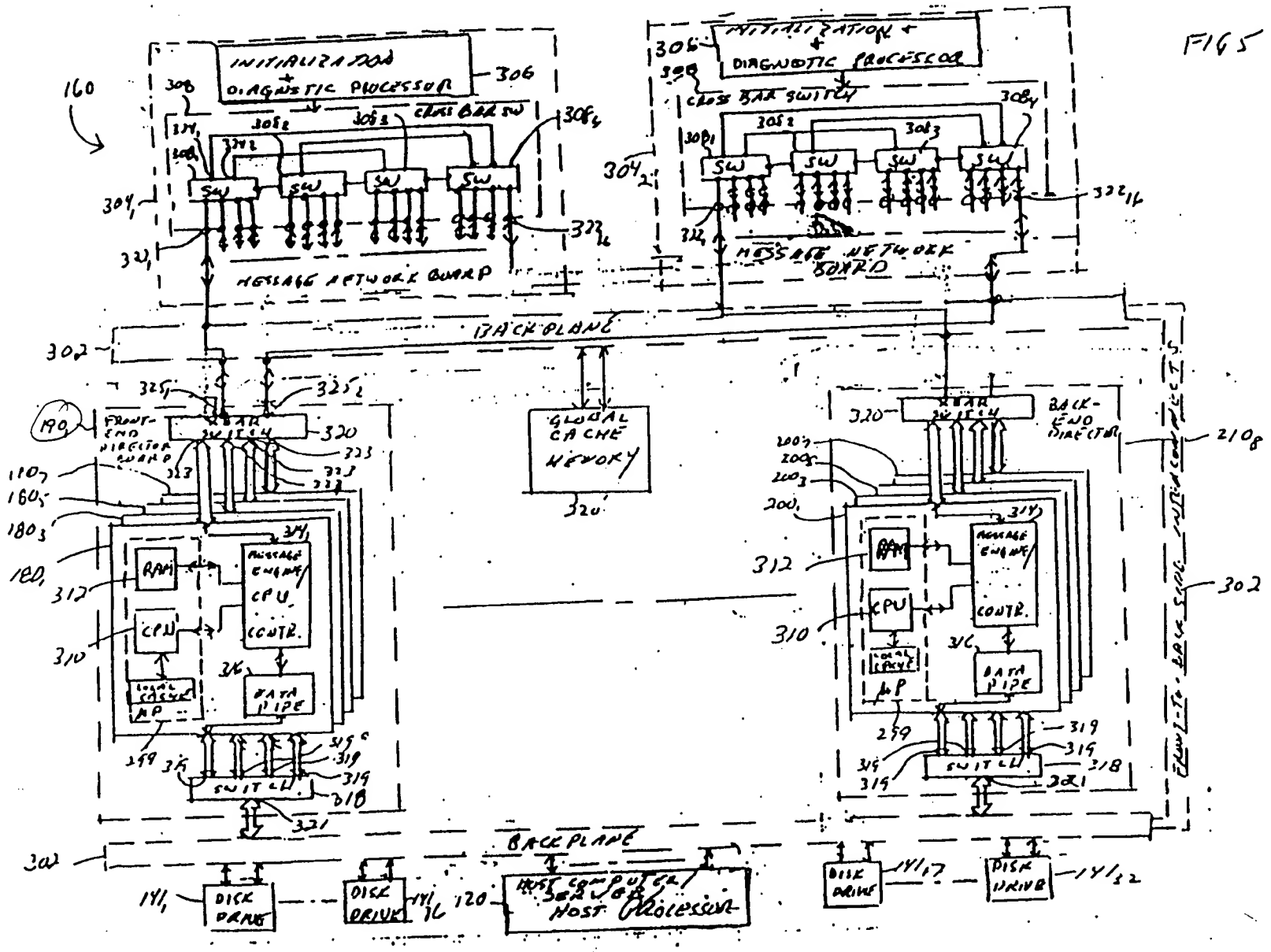


FIG 5

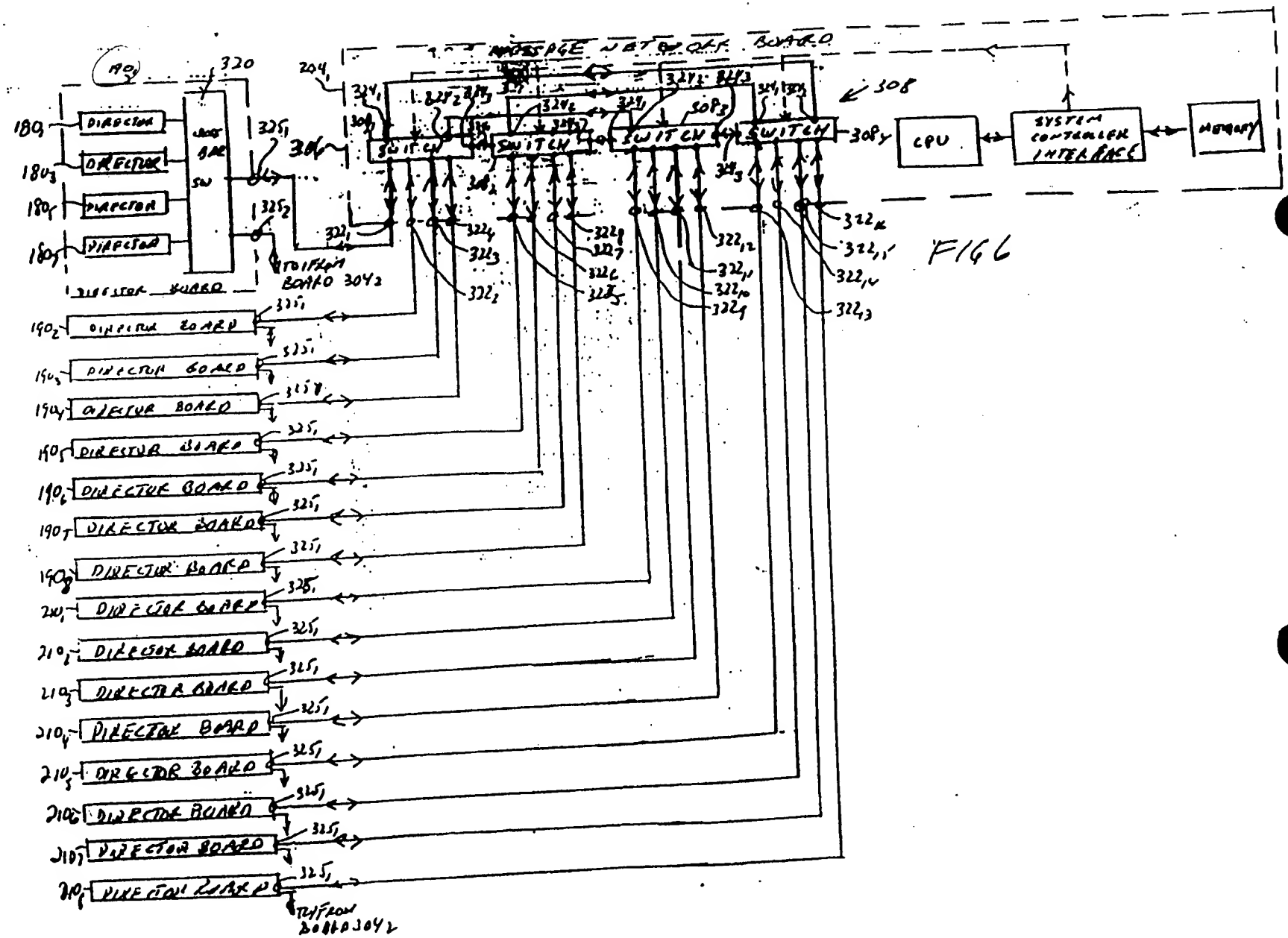
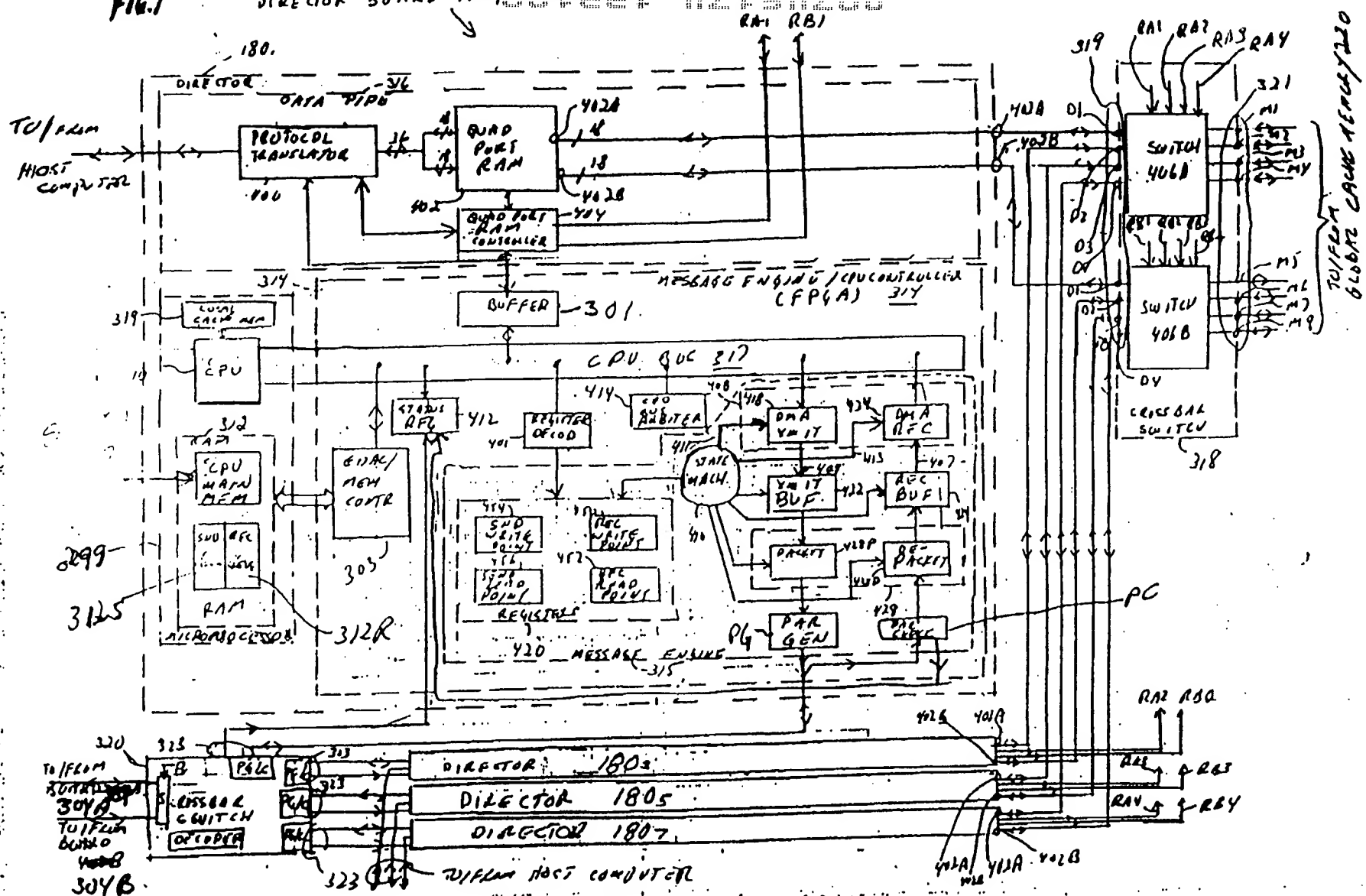

INTERFACE NETWORK BOARD
SWITCH
SWITCH
SWITCH
SWITCH
CPU
SYSTEM CONTROLLER INTERFACE
MEMORY
DIRECTOR
DIRECTOR
DIRECTOR
DIRECTOR
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
TO/FROM BOARD 304₂
TO/FROM BOARD 304₂

FIG 6

FIG. 7


DIRECTOR BOARD 190
180
DIRECTOR
DATA PATH 306
TO/FROM HOST COMPUTER
PROTOCOL TRANSLATOR
QUAD PORT RAM
QUAD PORT RAM CONTROLLER
BUFFER 301
MESSAGE ENGINE / CPU CONTROLLER (FPGA) 314
CPU BUS 317
CPU
CPU MAIN MEM
DMA/MEM CONTR
STATUS REG
REGISTER DECOD
CPU ARBITER
DMA XMIT
DMA REC
STATE MACH.
XMIT BUF
REC BUF
PACKET
RE-PACKET
PAR GEN
REGISTERS
MESSAGE ENGINE 315
RAM
MICROPROCESSOR
SWITCH 406A
SWITCH 406B
CROSSBAR SWITCH 318
TO/FROM GLOBAL CACHE MEMORY 320
CROSSBAR SWITCH
DIRECTOR 1803
DIRECTOR 1805
DIRECTOR 1807
TO/FROM HOST COMPUTER
TO/FROM BUS 306B
304B
PC

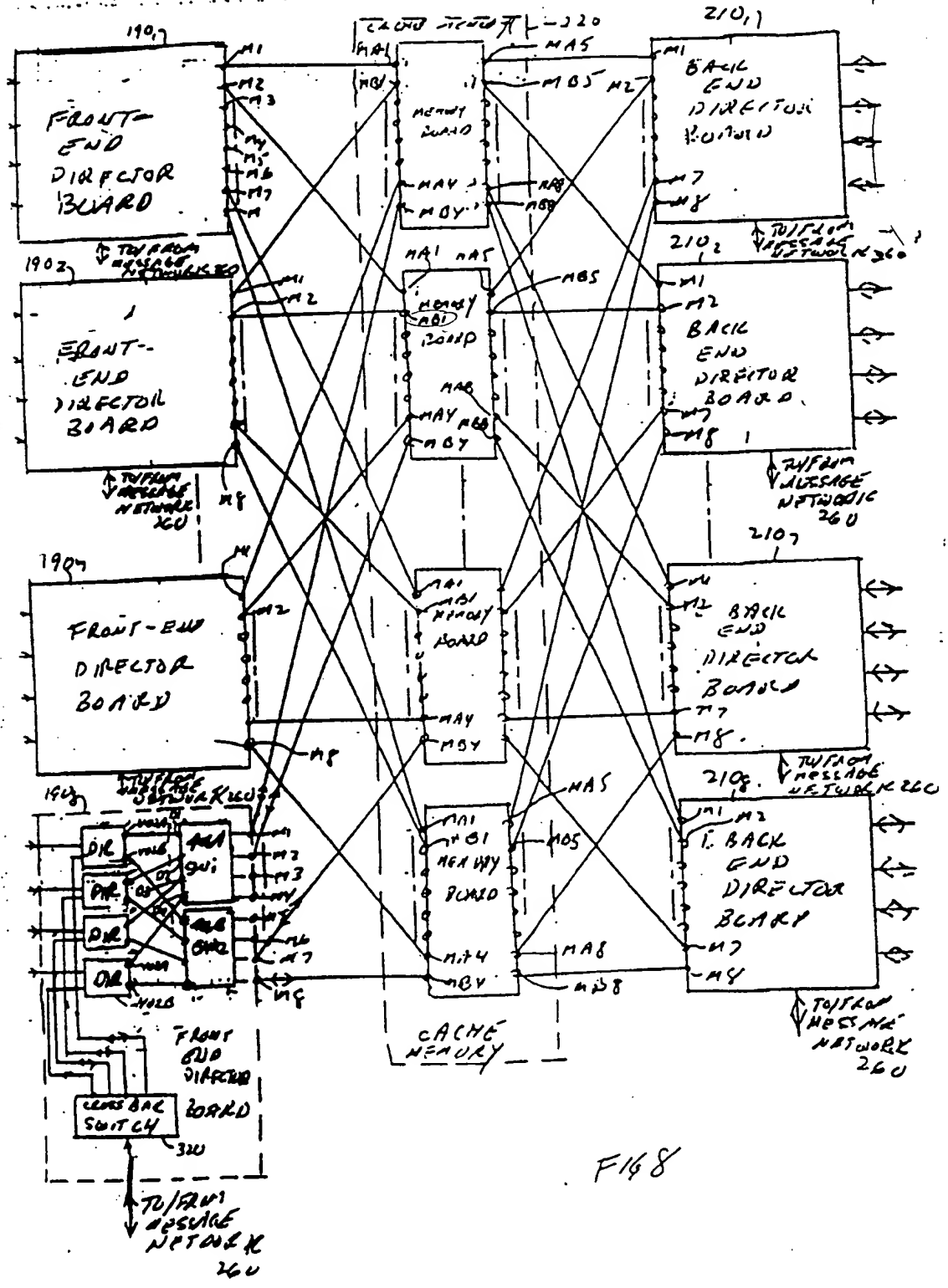
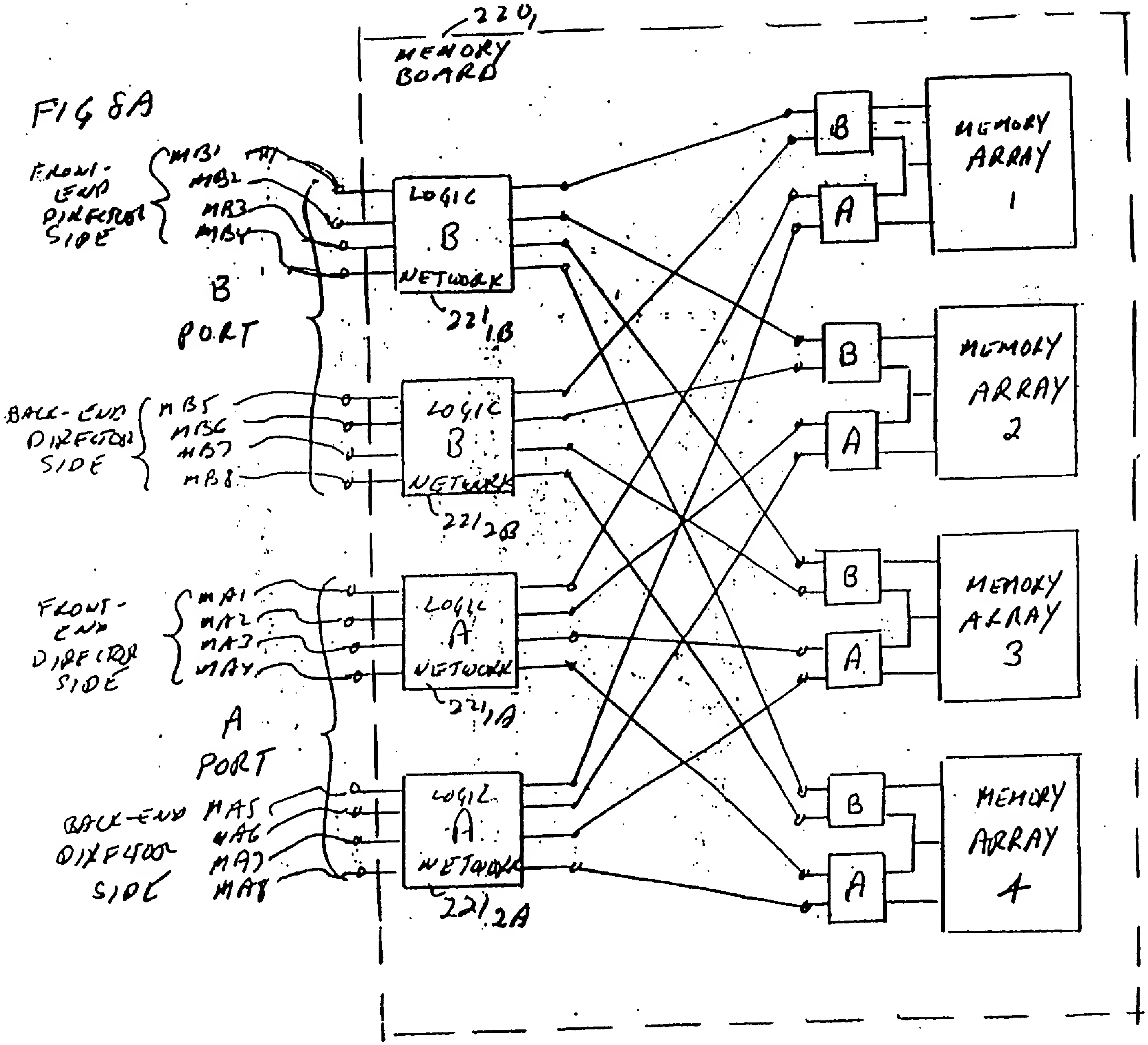

FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
MEMORY BOARD
MEMORY BOARD
MEMORY BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
SERVICE BAC SWITCH
FRONT END DIRECTOR BOARD
TO/FROM MESSAGE NETWORK 260

FIG 8

FIG 8A


220
MEMORY BOARD
MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4
B
A
LOGIC B NETWORK
221 1B
221 2B
LOGIC A NETWORK
221 1A
221 2A
FRONT-END DIRECTOR SIDE
MB1
MB2
MB3
MB4
B PORT
BACK-END DIRECTOR SIDE
MB5
MB6
MB7
MB8
MA1
MA2
MA3
MA4
A PORT
MA5
MA6
MA7
MA8

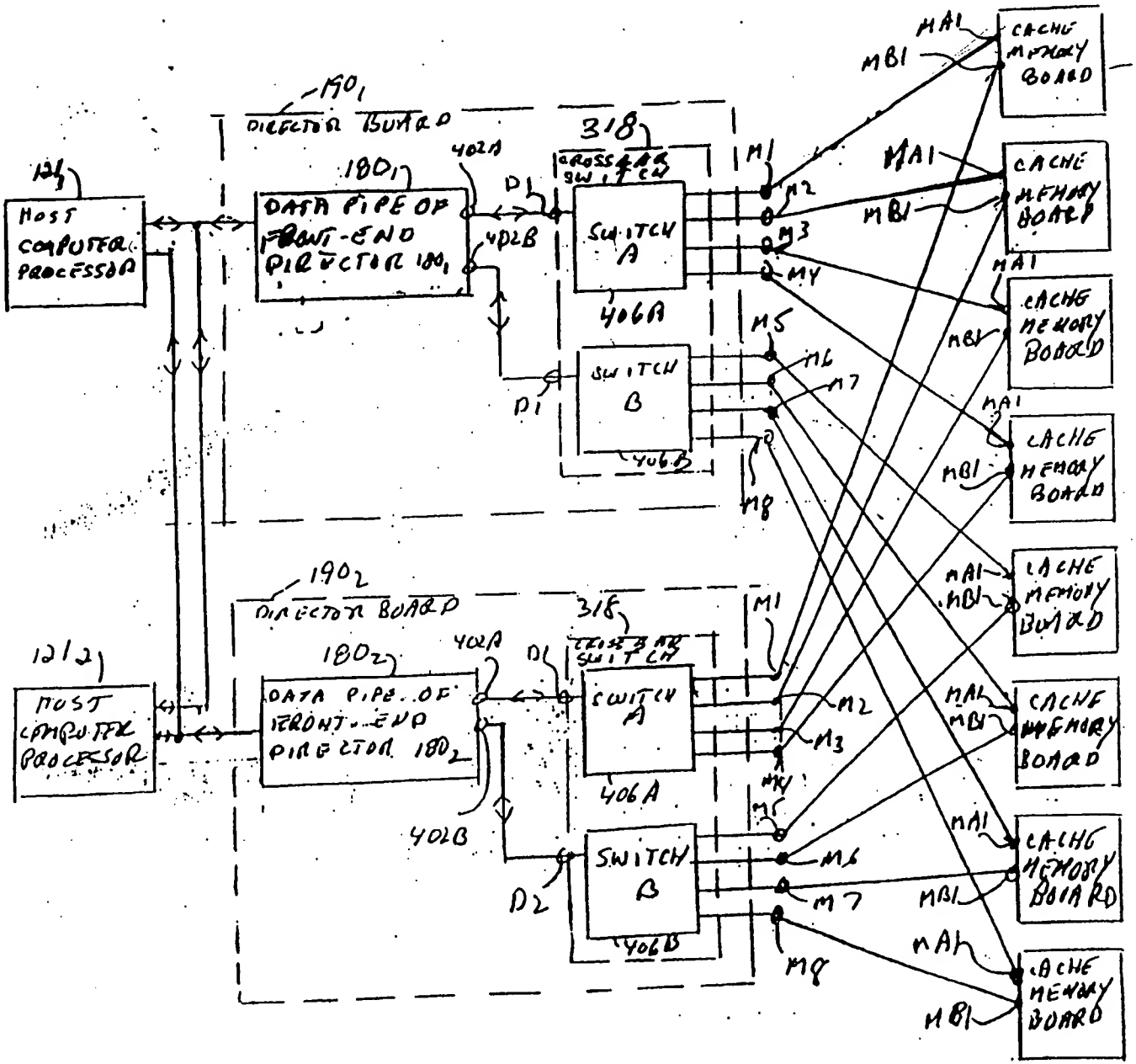

190₁
DIRECTOR BOARD
180₁
DATA PIPE OF FRONT-END DIRECTOR 180₁
HOST COMPUTER PROCESSOR
402A
402B
D1
318
CROSS BAR SWITCH
SWITCH A
SWITCH B
406A
406B
M1
M2
M3
M4
M5
M6
M7
M8
MA1
MB1
CACHE MEMORY BOARD
220₁
190₂
DIRECTOR BOARD
180₂
DATA PIPE OF FRONT-END DIRECTOR 180₂
HOST COMPUTER PROCESSOR
D2

FIG 8B

FIG. 9

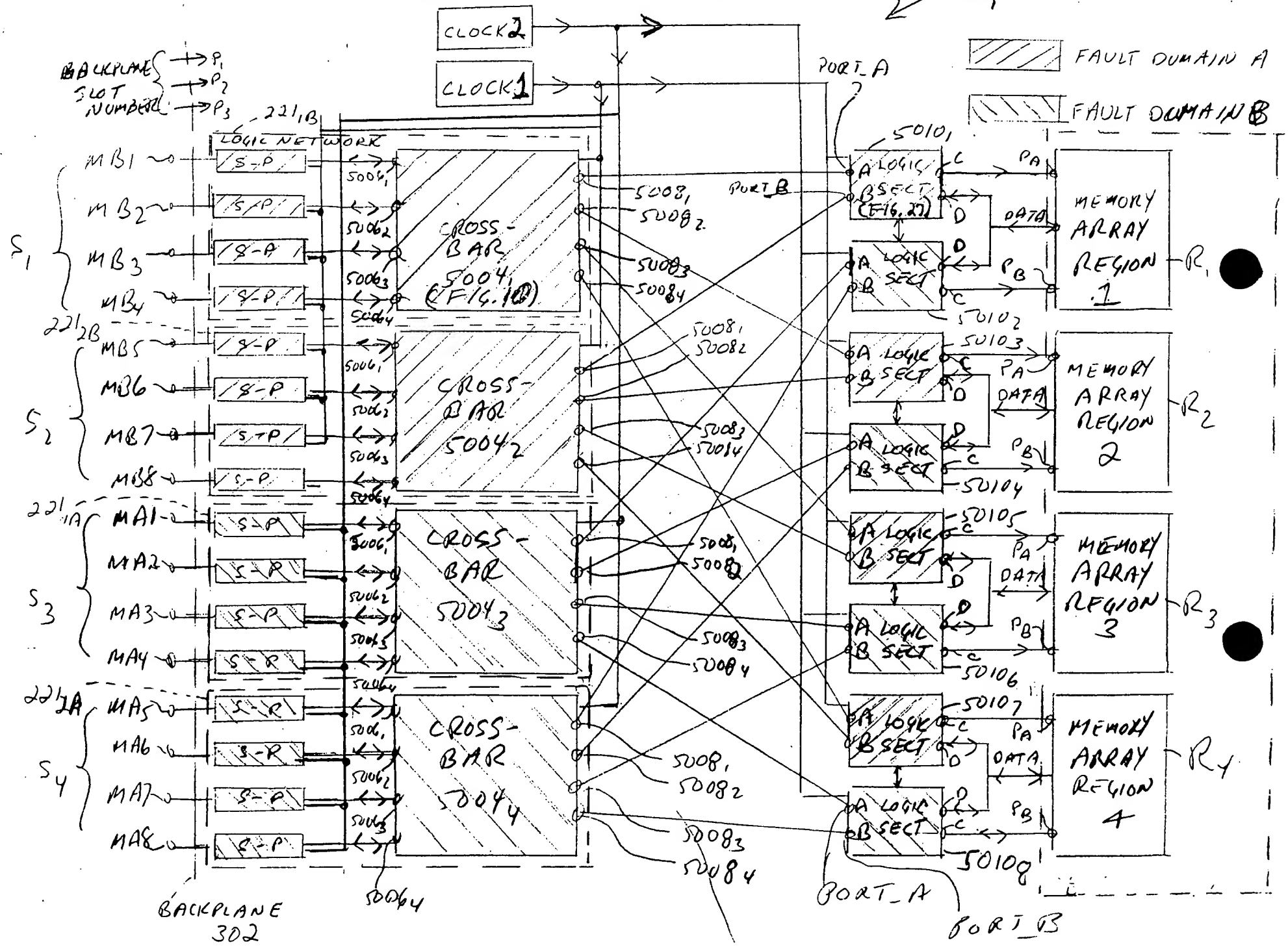
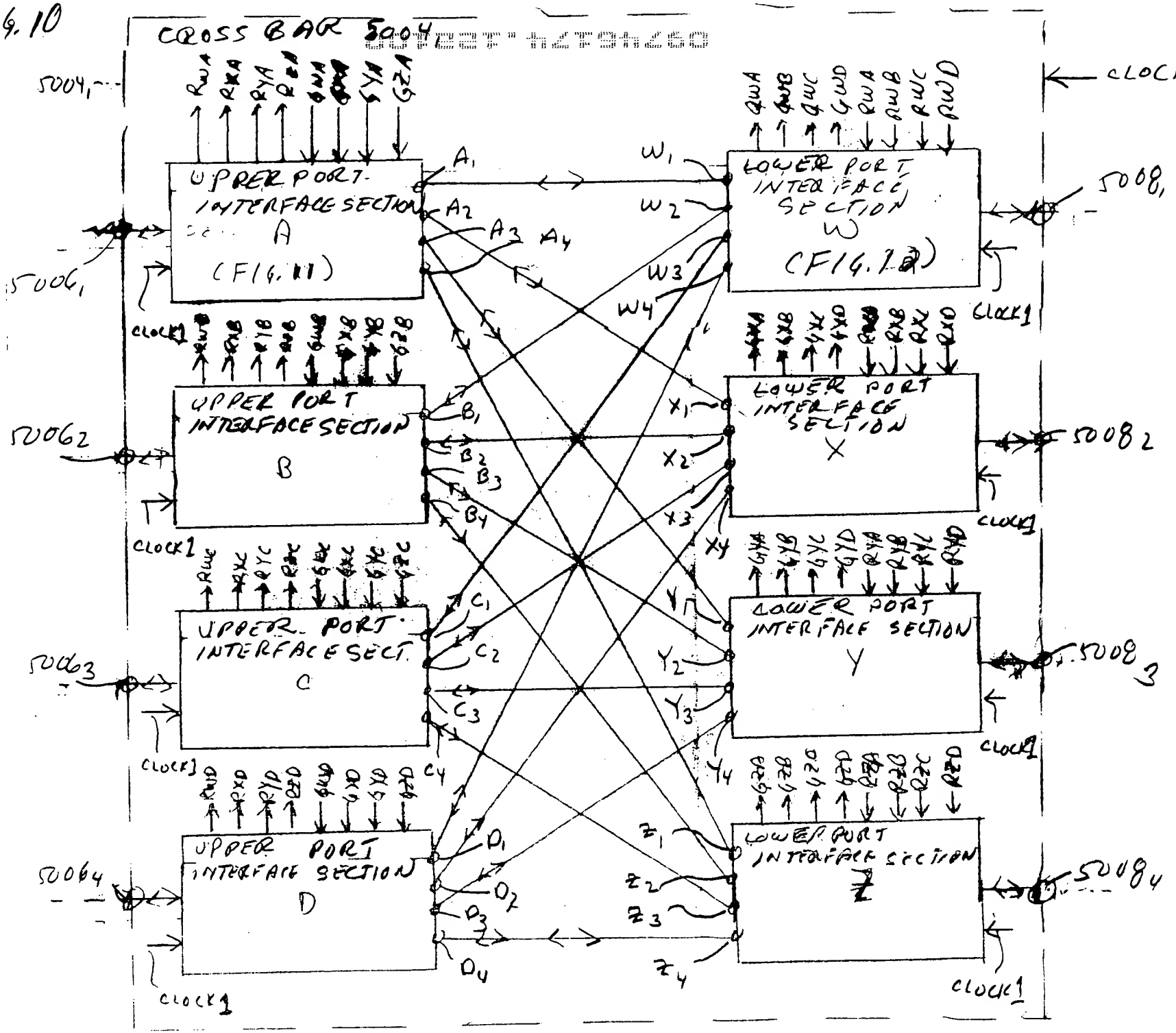

220₁
CLOCK 2
CLOCK 1
FAULT DOMAIN A
FAULT DOMAIN B
BACKPLANE SLOT NUMBER
P1
P2
P3
221₁B
LOGIC NETWORK
PORT_A
PORT_B
MB1
MB2
MB3
MB4
MB5
MB6
MB7
MB8
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
S-P
CROSS-BAR 5004
(FIG. 10)
CROSS-BAR 5004₂
CROSS-BAR 5004₃
CROSS-BAR 5004₄
5006₁
5006₂
5006₃
5006₄
5008₁
5008₂
5008₃
5008₄
5010₁
5010₂
5010₃
5010₄
5010₅
5010₆
5010₇
5010₈
A LOGIC
B SECT
(FIG. 27)
C
D
PA
PB
DATA
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
R1
R2
R3
R4
S1
S2
S3
S4
221₂B
221₁A
221₂A
BACKPLANE 302

FIG. 10


CROSS BAR 5004
5004₁
5006₁
5006₂
5006₃
5006₄
UPPER PORT INTERFACE SECTION A
(FIG. 11)
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECTION C
UPPER PORT INTERFACE SECTION D
LOWER PORT INTERFACE SECTION W
(FIG. 12)
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
5008₁
5008₂
5008₃
5008₄
CLOCK 1
A1
A2
A3
A4
B1
B2
B3
B4
C1
C2
C3
C4
D1
D2
D3
D4
W1
W2
W3
W4
X1
X2
X3
X4
Y1
Y2
Y3
Y4
Z1
Z2
Z3
Z4

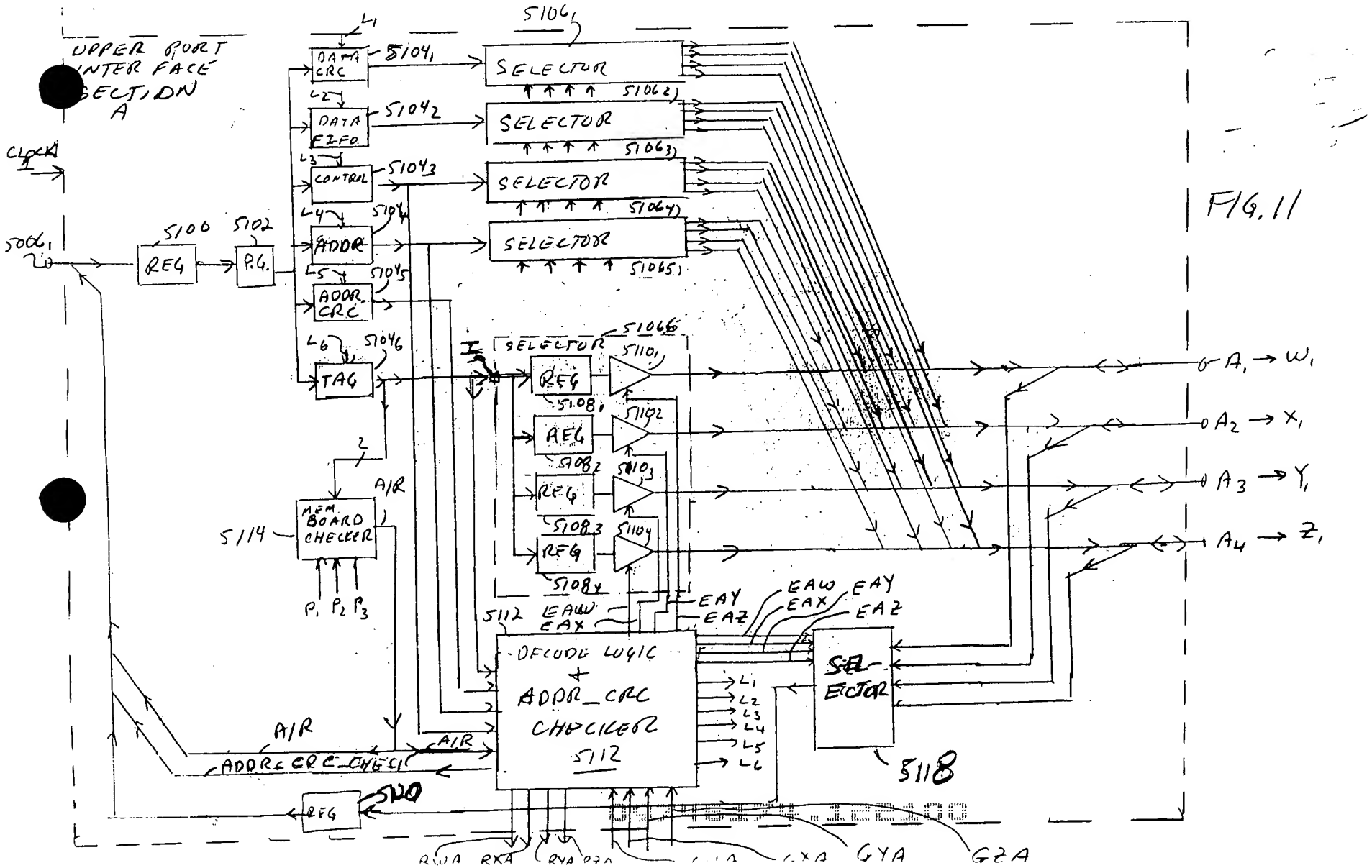

UPPER PORT INTER FACE SECTION A
CLOCK
5006₁
5100
REG
5102
P.G.
L1
DATA CRC
5104₁
L2
DATA FIFO
5104₂
L3
CONTROL
5104₃
L4
ADDR
5104₄
L5
ADDR CRC
5104₅
L6
TAG
5104₆
5106₁
SELECTOR
5106₂
SELECTOR
5106₃
SELECTOR
5106₄
SELECTOR
5106₅
SELECTOR
5106₆
5110₁
5110₂
5110₃
5110₄
REG
5108₁
REG
5108₂
REG
5108₃
REG
5108₄
A/R
MEM BOARD CHECKER
5114
P1 P2 P3
5112
DECODE LOGIC + ADDR_CRC CHECKER 5112
EAW EAX EAY EAZ
SELECTOR
5118
L1 L2 L3 L4 L5 L6
ADDR_CRC_CHECK
REG
5120
RXA RYA GYA GZA
A1 → W1
A2 → X1
A3 → Y1
A4 → Z1

FIG. 11

FIG. 12

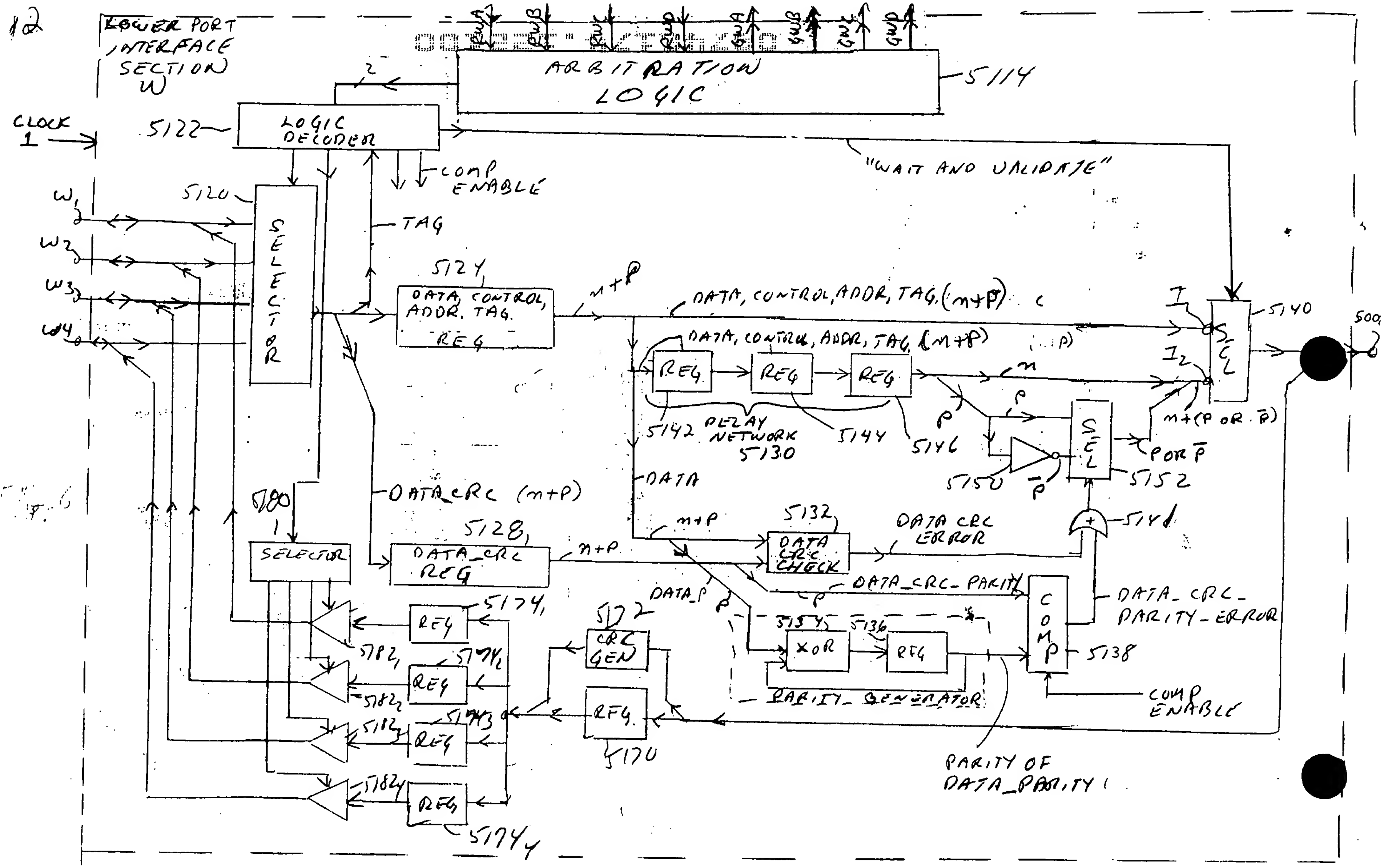
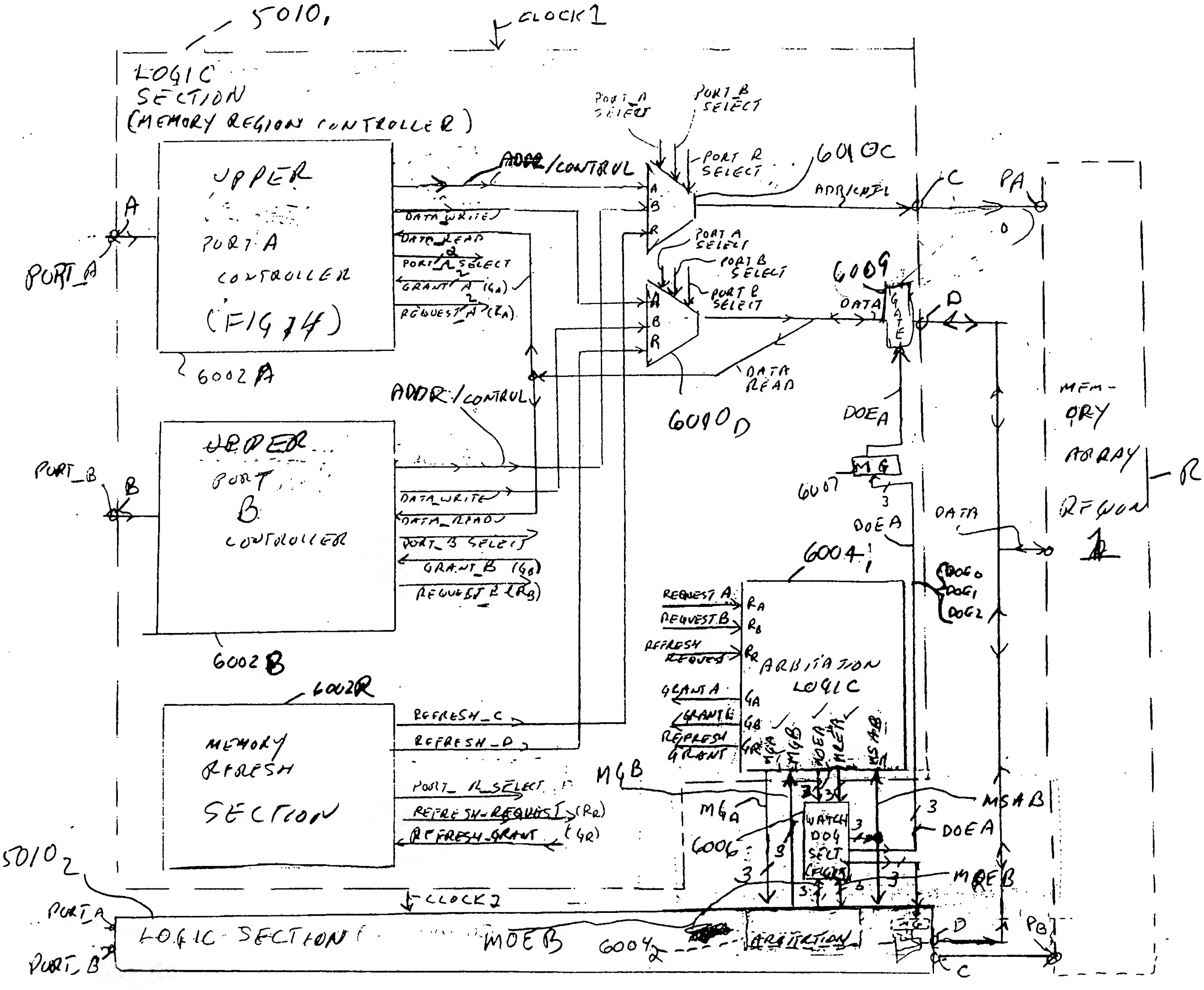

LOWER PORT INTERFACE SECTION W
CLOCK 1
ARBITRATION LOGIC
5114
LOGIC DECODER
5122
"WAIT AND VALIDATE"
COMP ENABLE
TAG
SELECTOR
5120
W1
W2
W3
W4
5124
DATA, CONTROL, ADDR, TAG. REG
m+P
DATA, CONTROL, ADDR, TAG, (m+P)
DATA, CONTROL, ADDR, TAG, (m+P)
REG
REG
REG
5142
DELAY NETWORK 5130
5144
5146
5140
SEL
I1
I2
500
m
P
SEL
5150
5152
P OR P̄
m+(P OR P̄)
DATA
DATA_CRC (m+P)
5180
SELECTOR
5128
DATA_CRC REG
m+P
5132
DATA CRC CHECK
DATA CRC ERROR
5148
DATA_CRC_PARITY
DATA_CRC_PARITY_ERROR
COMP
5138
DATA_P
5134
5136
XOR
REG
PARITY_GENERATOR
COMP ENABLE
PARITY OF DATA_PARITY
5172
CRC GEN
REG
5170
REG
REG
REG
REG
5174₁
5174₂
5174₃
5174₄
5182₁
5182₂
5182₃
5182₄

FIG. 13


5010₁
CLOCK 1
LOGIC SECTION (MEMORY REGION CONTROLLER)
UPPER PORT A CONTROLLER (FIG 14)
6002A
UPPER PORT B CONTROLLER
6002B
6002R
MEMORY REFRESH SECTION
PORT_A
PORT_B
ADDR/CONTROL
DATA_WRITE
DATA_READ
GRANT_A (GA)
REQUEST_A (RA)
DATA_WRITE
DATA_READ
PORT_B SELECT
GRANT_B (GB)
REQUEST_B (RB)
REFRESH_C
REFRESH_D
PORT_R_SELECT
REFRESH-REQUEST (RR)
REFRESH-GRANT (GR)
PORT_A SELECT
PORT_B SELECT
PORT R SELECT
6010C
6010D
ADDR/CNTL
DATA READ
6009
DATA
GATE
PA
PB
DOEA
MG
6007
6004₁
ARBITRATION LOGIC
REQUEST A
REQUEST B
REFRESH REQUEST
GRANT A
GRANT B
REFRESH GRANT
DOG0
DOG1
DOG2
MEMORY ARRAY REGION 1
R₁
MGB
MGA
MSAB
MOEB
6006
WATCH DOG SELECT (FIG 15)
5010₂
CLOCK 2
LOGIC SECTION
ARBITRATION
6004₂

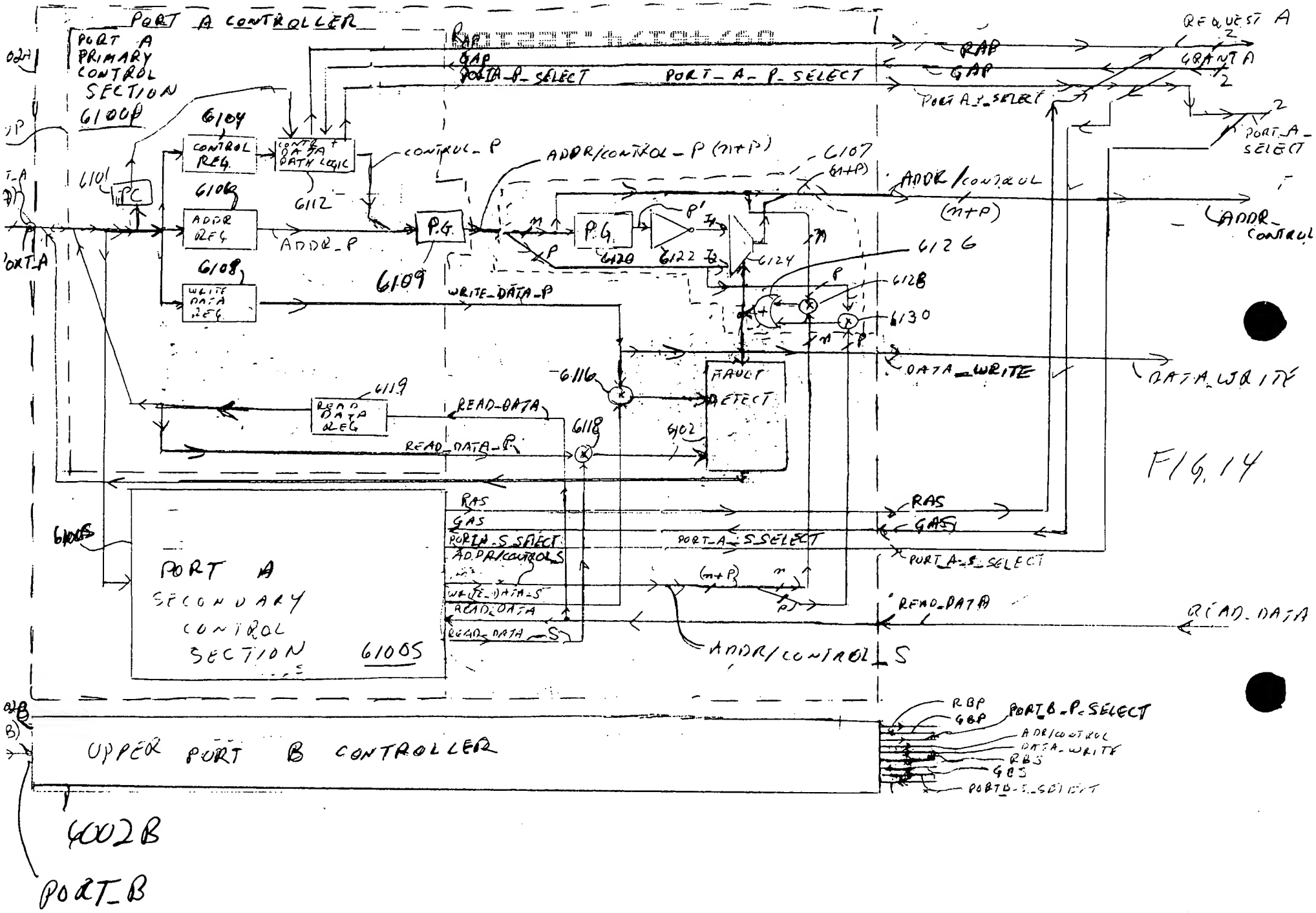
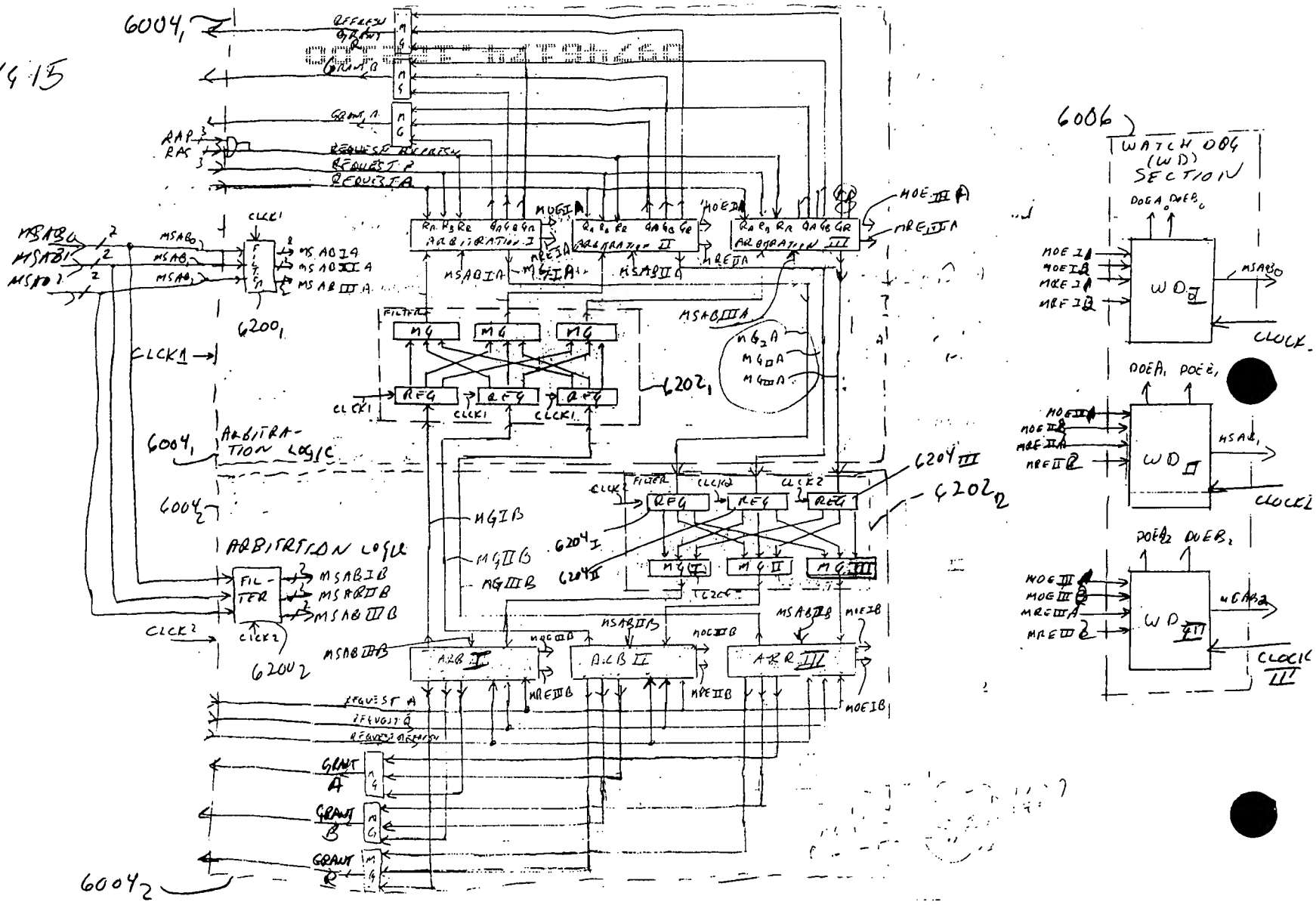

PORT A CONTROLLER
PORT A PRIMARY CONTROL SECTION 6100P
6104
CONTROL REG.
DATA PATH LOGIC
6101
PC
6106
ADDR REG.
6108
WRITE DATA REG.
6112
CONTROL_P
ADDR_P
6109
P.G.
ADDR/CONTROL_P (n+P)
6107
(n+P)
P.G.
6120
6122
6124
6126
6128
6130
WRITE_DATA_P
DATA_WRITE
6116
FAULT DETECT
6102
6119
READ DATA REG.
READ_DATA
READ_DATA_P
6118
RAS
CAS
PORT_A_S_SELECT
ADDR/CONTROL_S
WRITE_DATA_S
READ_DATA
READ_DATA_S
PORT A SECONDARY CONTROL SECTION 6100S
RAP
GAP
PORT_A_P_SELECT
REQUEST A
GRANT A
PORT_A_SELECT
ADDR/CONTROL (n+P)
ADDR_CONTROL
DATA_WRITE
RAS
CAS
PORT_A_S_SELECT
READ_DATA
ADDR/CONTROL_S
RBP
GBP
PORT_B_P_SELECT
ADDR/CONTROL
DATA_WRITE
RBS
GBS
PORT_B_S_SELECT
UPPER PORT B CONTROLLER
6002B
PORT_B

FIG. 14

FIG 15


6004₁
6004₂
6200₁
6200₂
6202₁
6202₂
6204 I
6204 II
6204 III
ARBITRATION LOGIC
ARBITRATION LOGIC
FILTER
REG
MG I
MG II
MG III
ARB I
ARB II
ARB III
GRANT A
GRANT B
GRANT R
CLCK1
CLCK2
6006
WATCH DOG (WD) SECTION
WD I
WD II
WD III
CLOCK
CLOCK II
CLOCK III

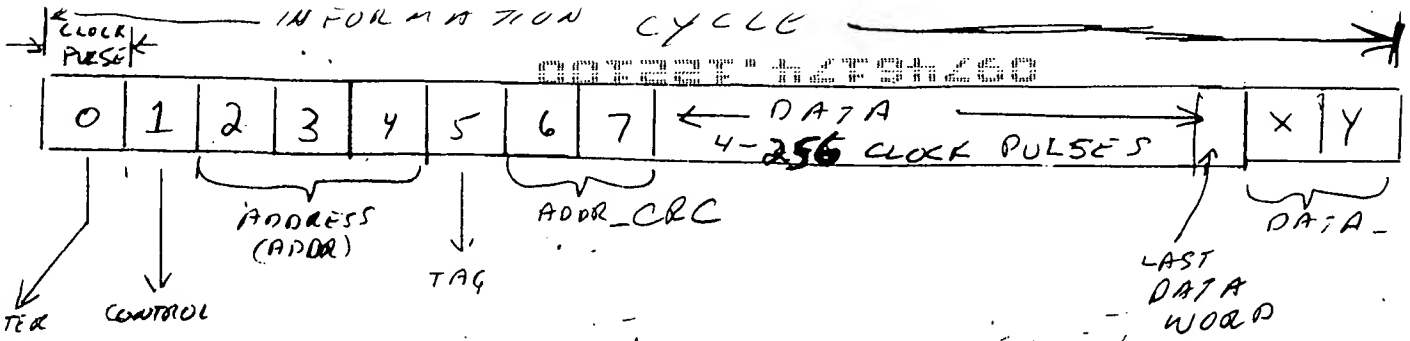


FIG. 16

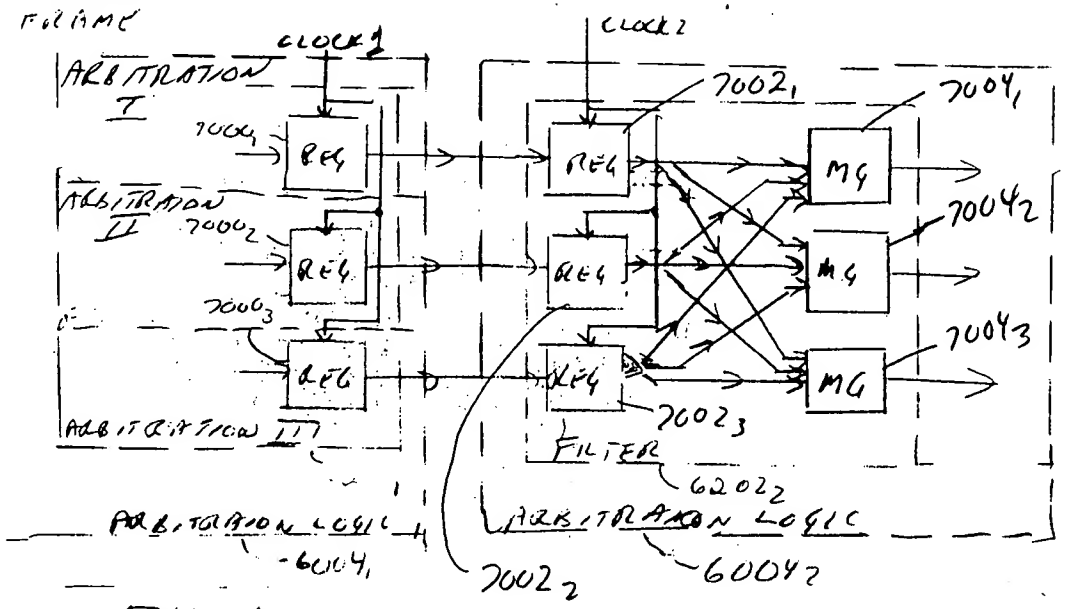


FIG. 18

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

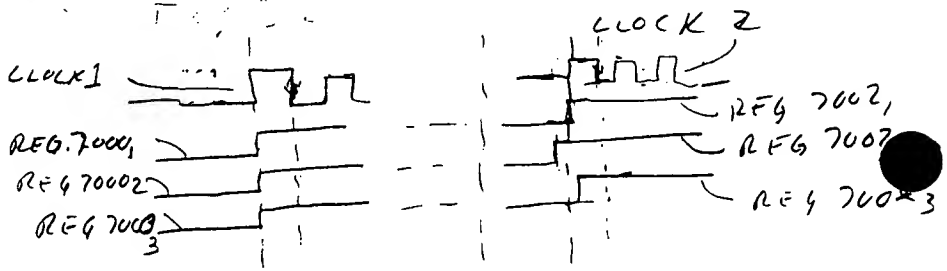


FIG. 19

FIG. 20